

Application Serial No. 10/701,326  
Reply to office action of December 23, 2005

PATENT  
Docket: CU-3430  
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**Amendments To The Claims**

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

**Listing of claims:**

1-3. (cancelled)

4. (currently amended) A chip stacked package comprising: The chip stacked package of Claim 3

a doubly down-set leadframe having a down-set tip to be wire-bonded;

a first semiconductor chip attached under the down-set tip of the

leadframe;

a first metal wire electrically connecting bonding pads of the first semiconductor chip with the down-set tip of the leadframe;

a second semiconductor chip attached on the leadframe;

a second metal wire electrically connecting the second semiconductor chip with the leadframe; and

an epoxy molding compound encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the leadframe while exposing the backside of the first semiconductor chip,

wherein the second semiconductor chip is attached by adhesives and

wherein the adhesives are filled in the entire space between the second semiconductor chip and the first semiconductor chip.

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5. (currently amended) A chip stacked package comprising: The chip-stacked package of Claim 3

a doubly down-set leadframe having a down-set tip to be wire-bonded;

a first semiconductor chip attached under the down-set tip of the leadframe;

a first metal wire electrically connecting bonding pads of the first semiconductor chip with the down-set tip of the leadframe;

a second semiconductor chip attached on the leadframe;

a second metal wire electrically connecting the second semiconductor chip with the leadframe; and

an epoxy molding compound encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the leadframe while exposing the backside of the first semiconductor chip,

wherein the second semiconductor chip is attached by adhesives and  
wherein the adhesives are interposed only between the second semiconductor chip and the leadframe.

6. (currently amended) The chip-stacked package of ~~Claim 4~~ Claim 4 wherein the second semiconductor chip is attached by means of an adhesive tape.

7. (currently amended) A chip-stacked package comprising:  
a doubly down-set leadframe having a down-set tip to be wire-bonded;

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a first semiconductor chip attached under the leadframe by means of a B-stage material interposed between the leadframe and the first semiconductor chip;

a first metal wire electrically connecting bonding pads of the first semiconductor chip with the tip of the leadframe;

a second semiconductor chip attached on the leadframe by means of adhesive;

a second metal wire electrically connecting the second semiconductor chip with the leadframe; and

an epoxy molding compound encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the leadframe while exposing the backside of the first semiconductor chip.

8. **(currently amended)** A chip-stacked package comprising:

a down-set leadframe having a tip to be wire-bonded, the tip being designed in such a manner as to have ~~a relatively small thickness~~ a thickness that is less than a thickness of a portion of the down-set leadframe adjacent to the tip;

a first semiconductor chip attached under the tip of the leadframe;

a first metal wire electrically connecting bonding pads of the first semiconductor chip with the tip of the leadframe;

a second semiconductor chip attached on the leadframe;

a second metal wire electrically connecting the second semiconductor chip with the leadframe; and

an epoxy molding compound encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the leadframe while exposing

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the backside of the first semiconductor chip.

9. (new) The chip-stacked package of Claim 4, wherein the first semiconductor chip is attached by means of an LOC tape.

10. (new) The chip-stacked package of Claim 5, wherein the first semiconductor chip is attached by means of an LOC tape.